Amendments to the Claims:

This listing of claims will replace all prior versions, all listings, of claims in the application:

Amendments to the Claims:

Claims 1 – 23 (cancelled)

24. (Currently Amended) A driving apparatus, comprising:

an output circuit to output a differential signal;

a reference current control circuit to provide a control voltage; and

a switch circuit, coupled to the output circuit and to the reference current control circuit, to selectively apply the control voltage, an operational voltage, and ground to the output circuit;

wherein a magnitude of the differential signal is determined based on at least one of a difference of the operational voltage and a first control voltage of the control voltage and a difference of a second control voltage of the control voltage and the ground.

25. (Currently Amended) The driving apparatus of claim 24,

wherein the output circuit comprises a first, a second, a third, and a fourth transistors;

wherein the magnitude of the differential signal is determined based on currents of the first, the second, the third, and the fourth transistors; the currents of the first and the second transistors are controlled by the difference of the operational voltage and the first control voltage; and the currents of the third and the fourth transistors are controlled by the difference of the second control voltage and the ground.

26. (Previously Presented) The driving apparatus of claim 25, wherein while the currents of the first and the fourth transistors are generated, the second and the third transistors are OFF, and while the first and the fourth transistors are OFF, the currents of the second and the third transistors are generated.

27. (Previously Presented) The driving apparatus of claim 25, wherein while the output circuit outputs the differential signal, the at least one of the first, the second, the third, and the fourth transistors operates at a saturation region.

28. (Currently Amended) The driving apparatus of claim 24, wherein the output circuit comprises a first, a second, a third, and a fourth transistors, wherein the switch circuit further comprises:

a first switch to selectively provide a first control voltage signal of the control voltage to the first transistor;

a second switch to selectively provide a second control voltage signal of the control voltage to the third transistor;

a third switch to selectively provide the first control voltage signal to the second transistor; [[and]]

a fourth switch to selectively provide the second control voltage signal to the fourth transistor;

a fifth switch to selectively provide the operational voltage to the first transistor;

a sixth switch to selectively provide the ground to the third transistor;

a seventh switch to selectively provide the operational voltage to the second transistor; and

an eighth switch to selectively provide the ground to the fourth transistor.

29. (Previously Presented) The driving apparatus of claim 28, further comprising: a switch control circuit to control the operation of the first, the second, the third, the fourth, the fifth, the sixth, the seventh, and the eighth switches.

30. (Previously Presented) The driving apparatus of claim 24, wherein the output circuit comprises a first, a second, a third, and a fourth transistors, and while the output circuit outputs the differential signal, the at least one of the first, the second, the third, and the fourth transistors operates at a saturation region.

31. (Previously Presented) The driving apparatus of claim 30, wherein the driving

apparatus is a low voltage differential signaling (LVDS) driving apparatus.

32. (Previously Presented) A driving apparatus comprising:
an output circuit to output a differential signal, the output circuit comprising a first, a second, a third, and a fourth transistors; and
a reference current control circuit to provide a control voltage to the output circuit such that a magnitude of the differential signal is determined based on the control voltage;
wherein while the output circuit outputs the differential signal, the at least one of the first, the second, the third, the fourth transistors operates at a saturation region.

33. (Previously Presented) The driving apparatus of claim 32, wherein the first and the second transistors are directly coupled to an operational voltage source.

34. (Previously Presented) The driving apparatus of claim 33, wherein the third and the fourth transistors are directly coupled to ground.

35. (Previously Presented) The driving apparatus of claim 32, wherein the first and the second transistors are PMOS transistors, and the third and the fourth transistors are NMOS transistors.

36. (Currently Amended) The driving apparatus of claim 32, wherein currents of the first and the second transistors are controlled by the difference of the operational voltage and a first control voltage of the control voltage.

37. (Currently Amended) The driving apparatus of claim 36, wherein currents of the third and the fourth transistors are controlled by the difference of a second control voltage of the control voltage and the ground.

38. (Currently Amended) An output circuit for outputting a differential signal, comprising:

a first transistor, directly coupled to an operational voltage, having a first gate for selectively receiving a first control signal or a third control signal;

a second transistor, directly coupled to the operational voltage, having a second gate for selectively receiving the first control signal or the third control signal;

[[and]]

a third transistor, coupled to the first transistor and directly coupled to ground, having a third gate for selectively receiving a second control signal or a fourth control signal; and

a fourth transistor, coupled to the second transistor and directly coupled to the ground, having a fourth gate for selectively receiving the second control signal or the fourth control signal.

39. (Previously Presented) The output circuit of claim 38, wherein a magnitude of the differential signal is determined according to a difference of the operational voltage and the first control voltage.

40. (Previously Presented) The output circuit of claim 39, wherein the magnitude of the differential signal is determined according to a difference of the second control voltage and the ground.

41. (Previously Presented) The output circuit of claim 38, wherein a magnitude of the differential signal is determined according to at least one of the first and the second control signals.

42. (Previously Presented) The output circuit of claim 41, wherein while the output circuit outputs the differential signal, at least one of the first, the second, the third, and the fourth transistors operates at a saturation region.

43. (Previously Presented) The output circuit of claim 41, wherein the third control voltage is the operational voltage and the fourth control voltage is the ground.